This listing of claims replaces all prior versions and listings of the claims in the application.

In the Claims

1. (canceled)

2. (currently amended) The method according to claim ~~1~~ 15 wherein said first FET is ~~an n-type~~a p-type FET (~~NFET~~PFET) and said second FET is ~~a p-type~~an n-type FET (~~PFET~~NFET).

3. (original) The method according to claim 2 wherein said gate stacks of said first and second FETs are aligned end-to-end in a horizontal direction over said substrate.

4. (currently amended) The method according to claim ~~1~~ 15 wherein said substrate is a silicon-on-insulator substrate having an upper layer including a single-crystal semiconductor.

5. (original) The method according to claim 4 wherein said single-crystal semiconductor consists essentially of silicon.

6. (original) The method according to claim 2 further comprising forming a self-aligned silicide aligned to said source and drain regions of said NFET and said PFET.

7. (original) The method according to claim 6 further comprising forming source and drain extensions of said NFET aligned to said gate stack of said NFET.

8. (original) The method according to claim 7 further comprising forming a thin dielectric on said gate stack of at least said PFET and forming source and drain extensions of said PFET aligned to said thin dielectric.

9. (original) The method according to claim 8 wherein said thin dielectric is formed by local thermal oxidation.

10. (original) The method according to claim 2 wherein said etching is performed by a process including a reactive ion etch.

11. (original) The method according to claim 10 wherein said first spacers consist essentially of silicon nitride and said second spacers consist essentially of silicon dioxide.

12. (original) The method according to claim 10 wherein said first spacers consist essentially of silicon dioxide and said second spacers consist essentially of silicon nitride.

13. (original) The method according to claim 6 wherein said silicide is a silicide of cobalt.

14. (original) The method according to claim 13 further comprising forming a self-aligned silicide aligned to said gate stacks of said NFET and said PFET.

15. (currently amended) A method of ~~defining spacings between the gates of~~ fabricating first and second field effect transistors (FETs) of an integrated circuit such that said first FET has different spacings between the gate and the source and drain regions thereof~~, the spacings differing in width between a first FET and a~~ than said second FET, comprising:

forming a first gate stack and a second gate stack overlying a main surface of a substrate;

forming ~~a~~ first ~~spacer~~ spacers and second spacers on each of said first and second gate stacks, each of said first ~~spacer~~ spacers having an "L" shape, each said first spacer including a vertically extending portion oriented in a vertical direction generally perpendicular to said main surface, and a horizontally extending portion oriented in a horizontal direction parallel to said main surface, said horizontally extending portion having an edge horizontally displaced from a wall of said vertically extending portion, ~~;~~

each of said second spacers extending along said walls of said vertically extending portions, said second spacers overlying said horizontally extending portions of said first spacers;

~~forming~~ implanting source and drain regions of said first FET aligned to said edges of said horizontally extending portions of said first ~~spacer~~ spacers of said first

gate stack;

removing said second spacers and said horizontally extending ~~portion~~ portions of said first ~~spacer~~ spacers by an anisotropic vertical etch process after forming said source and drain regions of said first FET; and

~~forming~~ implanting source and drain regions of said second FET in said substrate aligned to said walls of said vertically extending ~~portion~~ portions of said first ~~spacer~~ spacers of said second gate stack after removing said horizontally extending portions.

16-19. (canceled)

20. (withdrawn) An integrated circuit, comprising:

a first field effect transistor (FET) and a second FET, said first FET having source and drain regions each spaced a first distance from a first gate stack of said first FET, said second FET having source and drain regions each spaced a second distance from a second gate stack of said second FET, wherein said first and second distances differ by the width of a horizontally extending portion of a spacer disposed on a sidewall of one of said first and second gate stacks.